



BUK9K25-40E

Dual N-channel 40 V, 29 mΩ logic level MOSFET

10 December 2013

Product data sheet

1. General description

Dual logic level N-channel MOSFET in an LFAK56D (Dual Power-SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Dual MOSFET
- Q101 Compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with $V_{GS(th)}$ rating of greater than 0.5 V at 175 °C

3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	40	V
I_D	drain current	$V_{GS} = 5\text{ V}; T_{mb} = 25\text{ °C}; \text{Fig. 1}$	-	-	18.2	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 2}$	-	-	32	W
Static characteristics FET1 and FET2						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 5\text{ A}; T_j = 25\text{ °C}; \text{Fig. 11}$	-	24	29	mΩ
Dynamic characteristics FET1 and FET2						
Q_{GD}	gate-drain charge	$I_D = 5\text{ A}; V_{DS} = 32\text{ V}; V_{GS} = 5\text{ V}; T_j = 25\text{ °C}; \text{Fig. 13}; \text{Fig. 14}$	-	2.4	-	nC

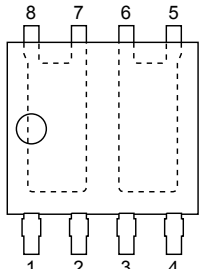
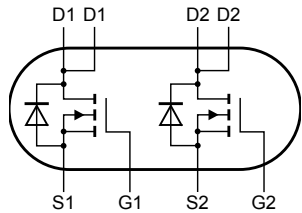


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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 <p>LFPAK56D (SOT1205)</p>	 <p><i>mbk725</i></p>
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK9K25-40E	LFPAK56D	Plastic single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9K25-40E	92540E

8. Limiting values

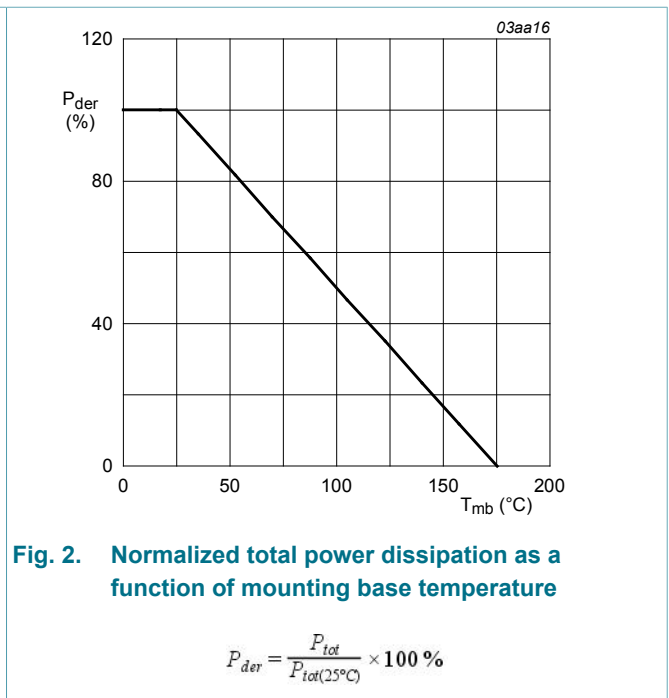
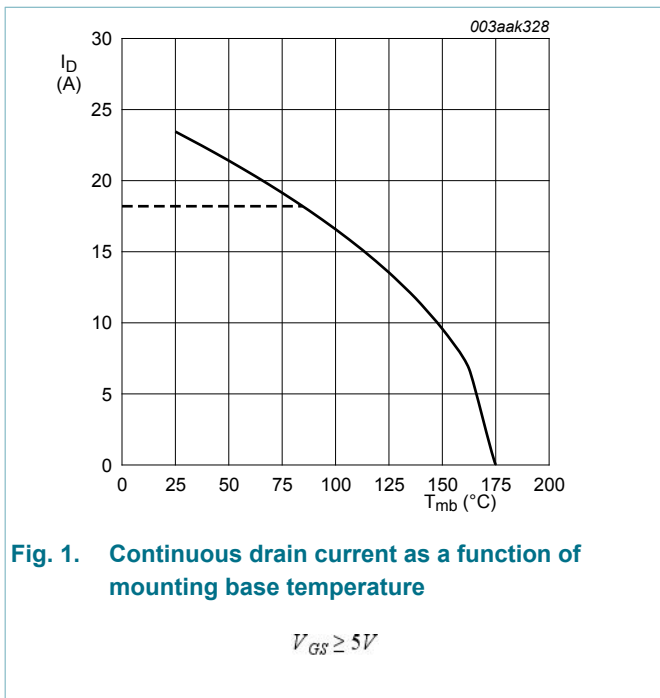
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	40	V	
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	40	V	
V_{GS}	gate-source voltage	$T_j \leq 175\text{ °C}$; Pulsed	[1][2]	-15	15	V
		$T_j \leq 175\text{ °C}$; DC		-10	10	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; Fig. 1	-	18.2	A	
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 5\text{ V}$; Fig. 1	-	16.6	A	
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Fig. 4	-	94	A	

Symbol	Parameter	Conditions	Min	Max	Unit
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 2	-	32	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
Source-drain diode FET1 and FET2					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	18.2	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	94	A
Avalanche Ruggedness FET1 and FET2					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 18.2\text{ A}$; $V_{sup} \leq 40\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; Fig. 3	[3][4]	-	15 mJ

- [1] Accumulated Pulse duration up to 50 hours delivers zero defect ppm.
- [2] Significantly longer life times are achieved by lowering T_j and or V_{GS} .
- [3] Refer to application note AN10273 for further information
- [4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C



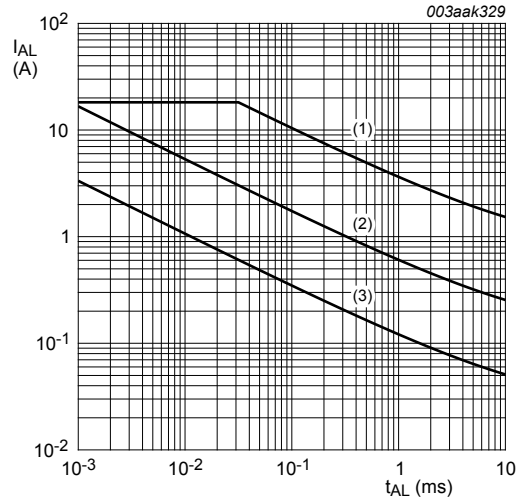


Fig. 3. Avalanche rating; avalanche current as a function of avalanche time

- (1) Single-pulse; $T_j = 25\text{ }^\circ\text{C}$.
- (2) Single-pulse; $T_j = 150\text{ }^\circ\text{C}$.
- (3) Repetitive.

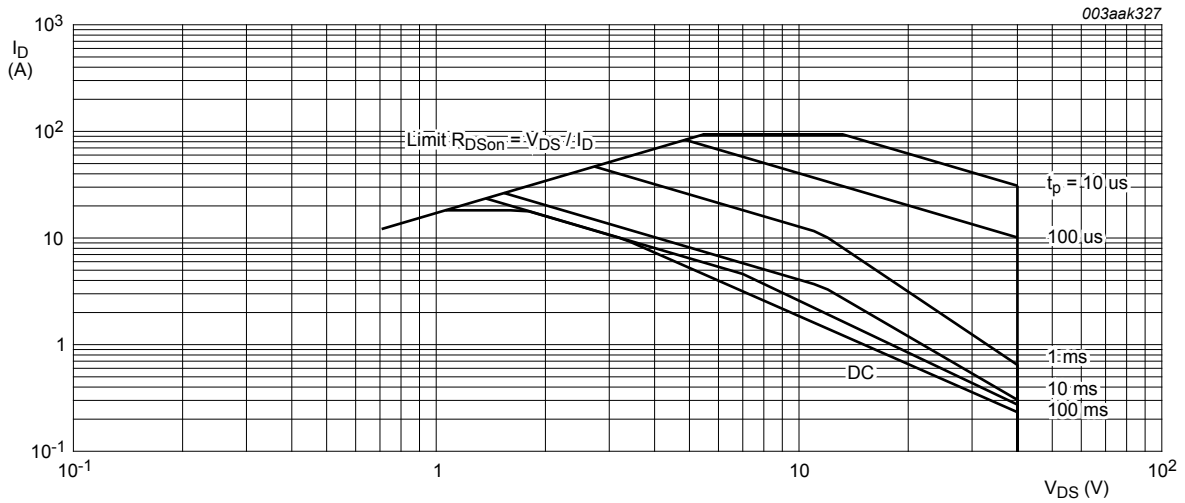


Fig. 4. Safe operating area; continuous and peak drain current as a function of drain-source voltage

$T_{mb} = 25\text{ }^\circ\text{C}$; I_{DM} is single pulse

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	4.68	K/W

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W

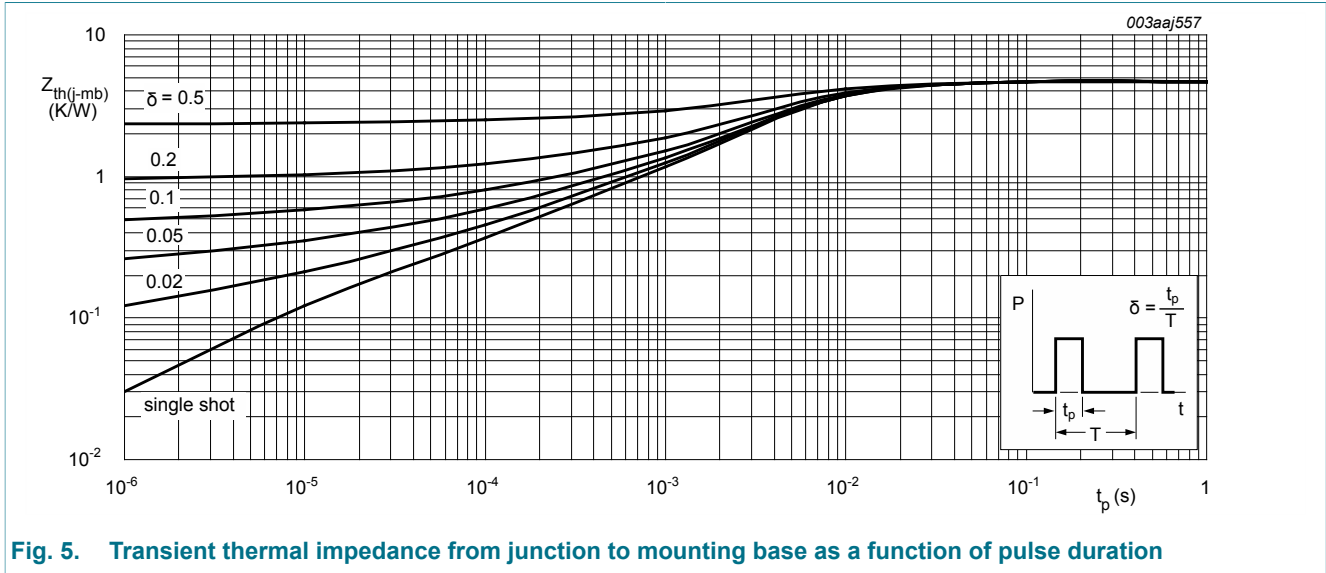


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics FET1 and FET2						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ Fig. 9; Fig. 10	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ Fig. 9; Fig. 10	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ Fig. 9; Fig. 10	-	-	2.45	V
I_{DSS}	drain leakage current	$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 \text{ }^\circ C$	-	-	500	μA
		$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.02	1	μA
I_{GSS}	gate leakage current	$V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5 V; I_D = 5 A; T_j = 25 \text{ }^\circ C;$ Fig. 11	-	24	29	mΩ
		$V_{GS} = 5 V; I_D = 5 A; T_j = 175 \text{ }^\circ C;$ Fig. 11; Fig. 12	-	48.2	58	mΩ
		$V_{GS} = 10 V; I_D = 5 A; T_j = 25 \text{ }^\circ C;$ Fig. 11	-	19	24	mΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics FET1 and FET2						
$Q_{G(\text{tot})}$	total gate charge	$I_D = 5 \text{ A}; V_{DS} = 32 \text{ V}; V_{GS} = 5 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C};$ Fig. 13 ; Fig. 14	-	6.3	-	nC
Q_{GS}	gate-source charge		-	1.4	-	nC
Q_{GD}	gate-drain charge		-	2.4	-	nC
C_{iss}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ Fig. 15	-	528	701	pF
C_{oss}	output capacitance		-	95	114	pF
C_{rss}	reverse transfer capacitance		-	56	76	pF
$t_{d(\text{on})}$	turn-on delay time	$V_{DS} = 32 \text{ V}; R_L = 6.4 \text{ } \Omega; V_{GS} = 5 \text{ V};$ $R_{G(\text{ext})} = 5 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}; I_D = 5 \text{ A}$	-	6.2	-	ns
t_r	rise time		-	9.2	-	ns
$t_{d(\text{off})}$	turn-off delay time		-	10.8	-	ns
t_f	fall time		-	8.9	-	ns
Source-drain diode FET1 and FET2						
V_{SD}	source-drain voltage	$I_S = 5 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 16	-	0.83	1.2	V
t_{rr}	reverse recovery time	$I_S = 5 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V};$	-	15.9	-	ns
Q_r	recovered charge	$V_{DS} = 20 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	7.6	-	nC

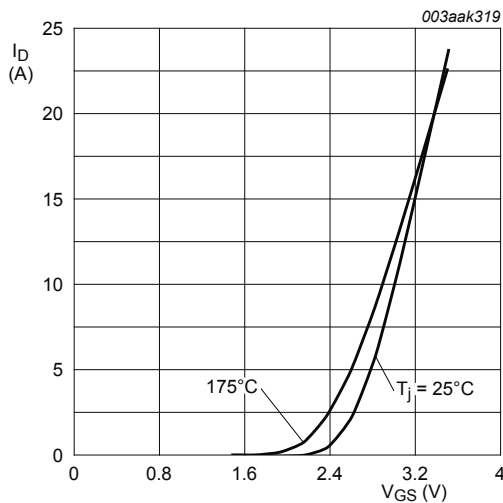


Fig. 6. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$$V_{DS} = 10V$$

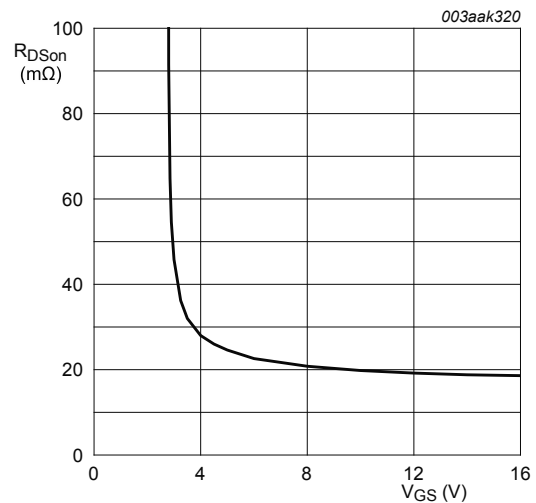
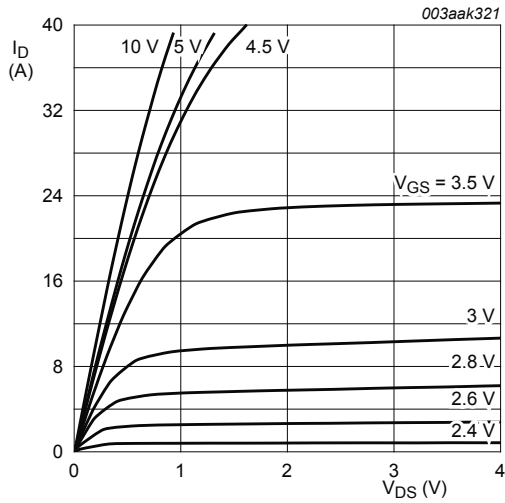


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$$T_j = 25^\circ\text{C}; I_D = 5A$$



$T_j = 25\text{ }^\circ\text{C}; t_p = 300\text{ }\mu\text{s}$

Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values

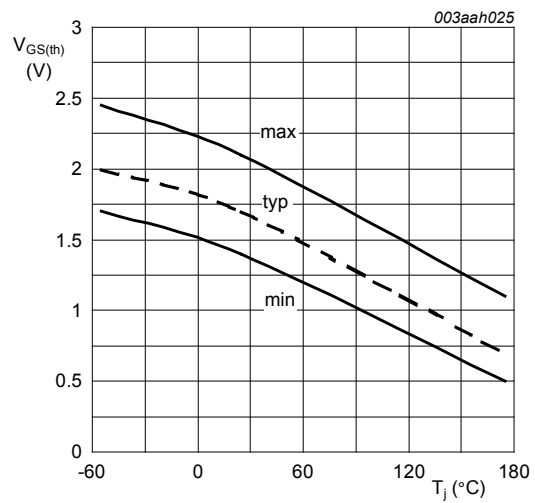


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

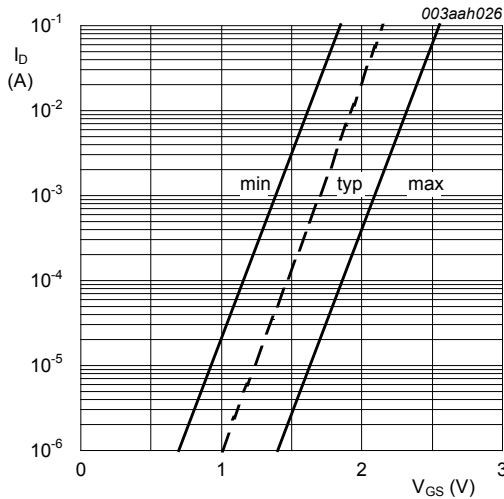
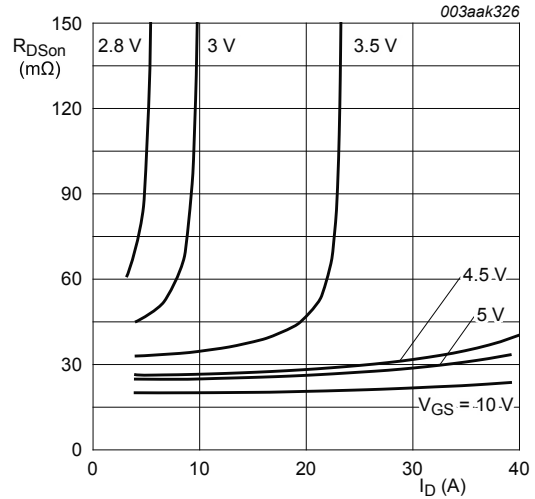


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 5\text{ V}$



$T_j = 25\text{ }^\circ\text{C}; t_p = 300\text{ }\mu\text{s}$

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

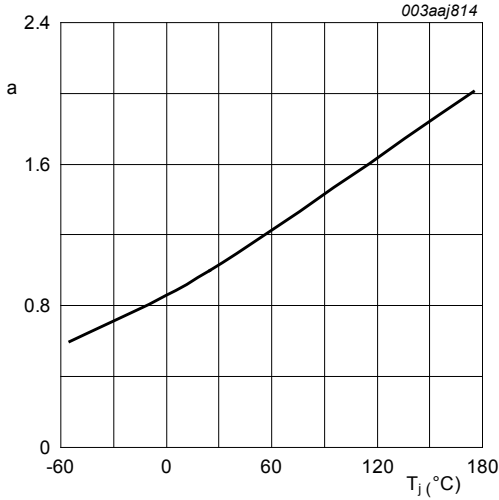


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)}(25^\circ\text{C})}$$

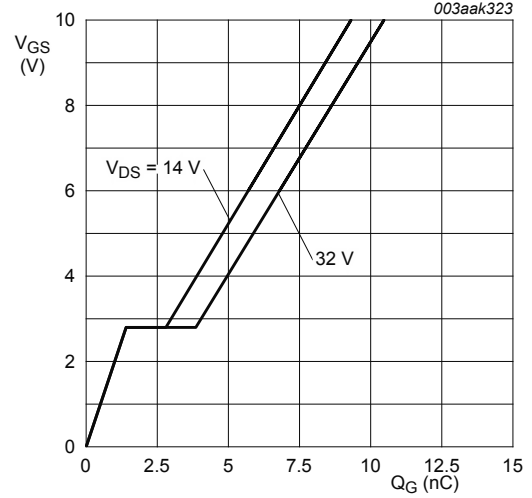


Fig. 13. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^\circ\text{C}; I_D = 5\text{ A}$



Fig. 14. Gate charge waveform definitions

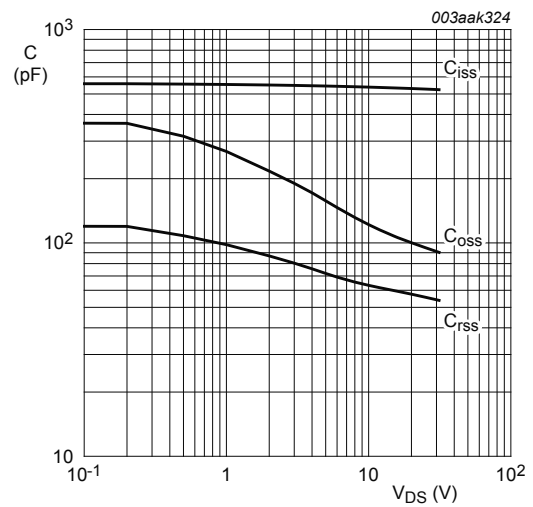


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

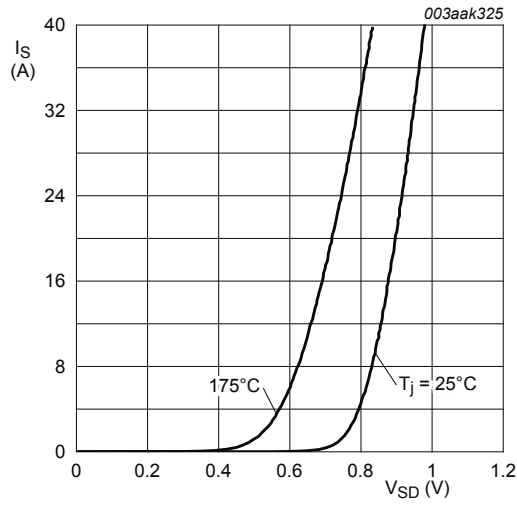
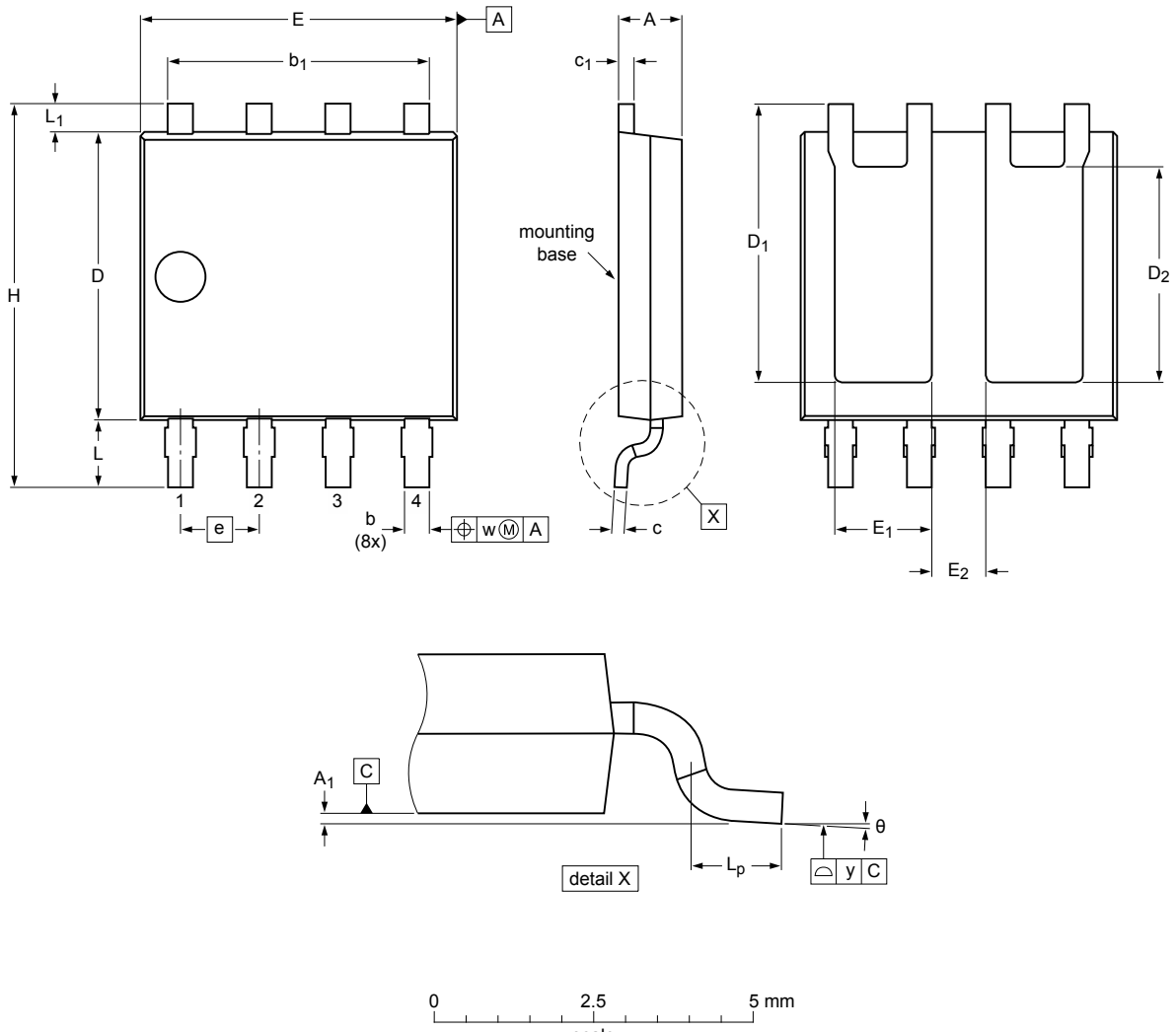


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0V$$

11. Package outline

Plastic single ended surface mounted package (LPAK56D); 8 leads SOT1205



Dimensions

Unit	A	A ₁	b	b ₁	c	c ₁	D ⁽¹⁾	D ₁ ⁽¹⁾	D ₂ ^(ref)	E ⁽¹⁾	E ₁ ⁽¹⁾	E ₂	e	H	L	L ₁	L _p	w	y	θ	
max	1.05	0.1	0.50	4.4	0.25	0.30	4.70	4.8	3.5	5.30	1.8	0.85	6.2	1.3	0.55	0.85		0.25	0.1	8°	
nom													1.27								
min		0.0	0.35	4.1	0.19	0.24	4.45			4.95	1.6		5.9	0.8	0.30	0.40				0°	

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot1205_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1205						13-02-19 13-02-21

Fig. 17. Package outline LPAK56D (SOT1205)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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